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EXAMINER
PHAM, BRENDA H

ART UNIT	PAPER NUMBER
2664	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/203,375	Applicant(s) WEGNER et al
	Examiner Brenda Pham	Art Unit 2664

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *THREE* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Dec 2, 1998*

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-25* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-25* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

1. Claims 1-25 have been examined.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 5, 17, 24 and 25 are rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

-Regarding claims 5 and 17, it is not clear what is meant by "DEVSEL#, C/BE#, STOP#, FRAME# and GNT# signals".

-Regarding claim 24, the recitation "An inter-bus communication system" does not have clear antecedent basis.

-Regarding claim 25, the recitation "A multiple bus system comprising the inter-bus communication system" does not have clear antecedent basis.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

5. Claims 1, 2, 6, 9-12, 14-15, 21-25 are rejected under 35 USC 102(e) as being anticipated by **Sherlock** (US 6,304,936).

-Regarding claims 1, 2, 13, 14 and 15, **Sherlock** discloses an apparatus and method of controlling the flow of data units across a bus bridge, comprising (referring to figure 13): detecting operational states of the bridge; disabling load access to the bridge when a first predefined operational state exists at the bridge; and enabling load access to the bridge when a second predefined operational state exists at the bridge.

Sherlock teaches "the bus bridge further includes a level-of-fullness monitor for monitoring the level of fullness of the common storage system in the multiple logical FIFO system. The level-of-fullness indications depending on the amount of storage capacity remaining in the common storage system at a given point in time. The system bus interface further comprises a flow control input and is operable to declare I/O halt and I/O resume commands, respectively, on the flow control input. The control circuitry issues the halt command when the first level-of-fullness indication is generated, and it issues the resume command when the second level-of-fullness indication is generated. Preferably, the first level-of-fullness indication is generated before the free storage capacity in the common storage system becomes less than a predetermined maximum size of post-halt cycle information that may come in through the system bus interface after an I/O halt condition is asserted. The second level-of-fullness indication may be generated after the amount of free storage capacity in the common storage system becomes greater than the predetermined maximum size of the post-halt cycle information.", (col. 2, lines 21-45).

-Regarding claim 6, **Sherlock** further teaches incrementing a counter when a data unit is loaded to the bridge.

Sherlock teaches "each write operation involving buffer system 900 will cause decode/gate block 1102 to increment one of write counters 0 to n-1, as determined by the value on write FIFO mum bus 904 when a pulse is applied to write enable signal 906.", (col. 10, lines 40-50).

-Regarding claim 9, **Sherlock** teaches incrementing and decrementing respectively in response to a data word as a data unit. (See col. 2, lines 53-67).

Sherlock teaches "When a word of write data is to be enqueued into a logical FIFO...When a word of read data is to be dequeued from a logical FIFO.."

-Regarding claims 10 and 21, **Sherlock** disabling the load access to the bridge (1300 of FIG. 13) by components on at least one bus (system bus 1306 of FIG. 13) when said counter reaches said predefined number. (See col. 12, lines 25-38).

-Regarding claims 11 and 22, **Sherlock** teaches wherein disabling includes disabling access to the bridge until a data unit is unloaded from the bridge.

Sherlock teaches "Whenever control block 1324 determines that there is only enough payload storage capacity remaining in system 100 to accommodate the worst case number of PIO cycles after an I/O halt command, control block 1324 issues an I/O halt command to system bus interface 1008 via flow control signal 1328. After a sufficient amount of payload storage capacity within system 100 has been freed by subsequent dequeueing of stored PIO cycle information, control block 1324 issues an I/O resume command to system bus interface 1008 via flow control signal 1328.", (col. 12, lines 25-35).

-Regarding claims 12 and 23, **Sherlock** teaches wherein disabling includes signaling at least one device (1308 of FIG. 13) on a bus (system bus 1306 of FIG. 13) in communication with the bus bridge (1300 of FIG. 13) to indicate that load access to the bridge will not be granted.

Sherlock teaches "Whenever control block 1324 determines that there is only enough payload storage capacity remaining in system 100 to accommodate the worst case number of PIO cycles after an I/O halt command, control block 1324 issues an I/O signal 1328 to system bus interface (1308).", (col. 12, lines 25-30).

-Regarding claims 24 and 25, **Sherlock** further teaches a bridge in communication with at least two data buses for transferring data between said at least two data buses (see figure 13, system bus 1306 and buses connected to I/O bus interface 1312-1316, and inter-bus (see figure 13).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3, 4 and 16 are rejected under 35 USC 103(a) as being unpatentable over **Sherlock** (US 6,304,936), in view of **David et al** (US 6,026,460), hereinafter referred to as **David**.

-Regarding claims 3, 4, and 16, as explained above in the rejection statement of claims 1 and 14, **Sherlock** discloses all the claim limitations recited in claims 1 and 14 (parent claims).

Sherlock does not teach monitoring activity/signal on each bus connected to the bridge. However these claimed features are well known in the art and disclosed by **David** in according to figure 2, items 260, 245).

David teaches "A method and apparatus for sequencing system bus grants and disabling a posting buffer in a bus bridge to improve bus efficiency...The bus bridge includes a bus activity monitor for monitoring bus cycles on a firs bus, and inbound posting buffer, and a control logic. The control logic indicates whether to grant control of the first bus to a first processor on the first

bus based on whether the inbound posting buffer is empty, and control disabling of posting to the inbound posting buffer.", (see abstract).

David further teaches "The PCI bus bridge 150 also includes a system bus activity monitor 245. The system bus activity monitor 245 continually monitors the system bus 110 for processor activity, monitoring the access.sub.--strobe signal and bus ownership signal on the system bus 110."

It would have been obvious to those having ordinary skill in the art at the time of the invention was made to implement the system bus activity monitor, such as that suggested by **David**, in **Sherlock** for constantly examine bus traffic and reconfigure bus agent connection points from one data bus to another.

8. Claims 8 and 19 are rejected under 35 USC 103(a) as being unpatentable over **Sherlock** (US 6,304,936), in view of **Duncan et al** (US 5,953,538), hereinafter referred to as **Duncan**.

-Regarding claims 8 and 19, as explained above in the rejection statement of claims 1 and 14, sherlock discloses all the claim limitations recited in claims 1 and 14 (parent claims).

Sherlock does not teach counter includes an ATM cell.

Duncan, in the same field of endeavor, teaches this limitation.

Duncan teaches "Upon completion of the DMA transfer, the CPU device would then issue an ATM Write/DMA read operation to transfer the data from memory 110 over the ATM adapter 108.", (col. 10, lines 60-65).

It would have been obvious to those having ordinary skill in the art at the time of the invention was made to implement ATM cell in Sherlock to provide data transfers between devices coupled to different network.

9. Claims 7, 18, 20 are rejected under 35 USC 103(a) as being unpatentable over **Sherlock** (US 6,304,936), in view of **Rozario et al** (US 6,173,378), hereinafter referred to as **Rozario**.

-Regarding claim 7, 18, and 20, as explained above in the rejection statement of claims 1 and 14, **Sherlock** discloses all the claim limitations recited in claims 1 and 14 (parent claims).

Sherlock shows in figure 11 that difference counters are used for determined the value of data unit loaded to the bridge and unloaded from the bridge, a subtractor is used for determines the difference between the value of write counter and the value of read counter. The difference value is then compared with threshold constants by comparators to generate the level-of-fullness in the buffer.

Sherlock teaches "each write operation involving buffer system 900 will cause decode/gate block 1102 to increment one of write counters 0 to n-1, as determined by the value on write FIFO mum bus 904 when a pulse is applied to write enable signal 906. Similarly, each read operation involving buffer system 900 will cause decode/gate block 1104 to increment one of read counters 0 to n-1, as determined by the value on read FIFO mum bus 908 when a pulse is applied to read enable signal 910...Finally, subtractor 1208 determines the difference between the value of write counter 1200 and the synchronized and converted value of read counter 1202. The difference value is then compared with threshold constants by comparators 1210-1214 to generate numerous different level-of-fullness indications.", (col. 10, 11, lines 40-67 and 1-20, respectively).

Although **Sherlock** does not teach a single counter is used for incremented by the bridge when a data unit is loaded to the bridge and decremented when a data unit is unloaded from the bridge, it is well known in the art that one or more counters which increment or decrement as access requests are written to and read from the buffer, and is suggested by **Rozario**, (see col. 6, lines 13-16).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to implement a single counter for determined the value of data unit load to the bridge and for determined the value of data unit unload from the bridge, in **Sherlock**. As a result, system processing time is shorter by eliminates some precessing steps and the used of one counter also contributes to reducing the hardware cost of the whole system.

Conclusion

10. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist)

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brenda Pham whose telephone number is (703) 308-0148. The examiner can normally be reached on Monday-Friday from 9:00 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin, can be reached on (703) 305-4366.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Brenda Pham
February 21, 2002

WELLINGTON CHIN
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